**September 2nd Register Senior Project Meeting**

**Dr. Pearlstein’s Office, 1:00-2:30**

**Members in Attendance:** Dr. Pearlstein, Zachary Nelson, and Julie Swift

* Project Goals Slide
  + Why are we doing this project?
    - This is not a common project for undergraduates because of the high cost associated with the fabrication of a chip.
    - Describe the MOSIS Education Service
    - Free fabrication for 3mm by 3mm
  + Also refer to this as VLSI
  + Explain the difference between an FPGA and an Integrated Circuit
  + Why did we choose to process audio as our application?
    - Complex and interesting enough
    - Not too hard so that this project is able to be completed
  + Take out parameterized filters
  + Put a picture of a chip
* Chip Overview Slide
  + I2S is digital but represents an analog signal
* DropBox is for confidential files while GitHub is for everything else
* I2C Slide
  + sda\_in and sda\_out are both interfaces
* Filter Slide
  + Fix the summation sign
* DFT Slide
  + We will most likely not be doing this task but it is good to have as background information.
* Gate Level Simulation
  + We will not do gate level simulation that intensively.
* Place and Route
  + We will not manually do the place and route, the EDA tools will do it for us.
  + We may be doing manual floor planning.
* Create a Block Level Testbenches Slide
  + We will have tb for each individual block as well as the overall chip
* Discussed interfaces for the register.v module
* Discussed a block diagram of the register.v module.
  + Ask Julie or Zach for more specifics
* MOSIS information
  + We can order one lot of 40 chips
  + We will fab using the Global Foundries 180 nm CMOS (7HV) process
  + MOSIS technology code for the 7HV process is GF\_7HV
  + Customer Submission date for 7HV is **March 7th, 2016**